REMARKS

Claims 1, 4, 8, 12, 15 and 16 have been amended and claims 18 to 27 have been canceled. Claims 1, 2, 4 and 6 to 16 and 28 remain active in this application.

Claims 4, 8, 12, 15 and 16 have been amended as kindly suggested to overcome the objections thereto.

Claims 1, 2, 4 and 6 to 28 were rejected under 35 U.S.C.102(e) as being anticipated by Koga (U.S. 6,191,615). The rejection is respectfully traversed.

Claim 1 now more clearly defines the invention and requires, among other features, a logic circuit, which includes a pair of complementary serially connected MOS transistors coupled between a voltage supply source and a reference voltage source, the transistor coupled to said reference voltage source having a normally higher threshold voltage and lower leakage and driving current than the normal threshold voltage and leakage current of the other of said complementary serially connected MOS transistors in the operational state. No such structure is taught or suggested by Koga either alone or in the combination as claimed.

Claim 1 further requires a bias voltage supply circuit which selectively supplies a first bias voltage in the operational state or a second bias voltage in the standby state which are different from each other to the substrate region of the other of the complementary serially connected MOS transistors with substantially no bias voltage supplied to the substrate region of said transistor coupled to said reference voltage source to raise the threshold voltage and diminish the leakage current of the other of said MOS transistors in the standby state. No such structure is taught or suggested by Koga either alone or in the combination as claimed. Note that N12 of Fig. 1 of Koga is not coupled to

ground of the circuit within the well would be a constant short circuit. Furthermore, even when transistors MN12 and MN 13 of Koga are conducting, there is still a voltage drop between N12 and ground via the transistors themselves.

Claims 2, 4, 6 and 7 depend from claim 1 and therefore define patentably over Koga for at least the reasons presented above with reference to claim 1.

In addition, claim 2 further limits claim 1 by requiring that the bias voltage supply circuit include a first MOS transistor connected between a first voltage supply line and a bias voltage supply line and a second MOS transistor connected between a second voltage supply line and the bias voltage supply line, and the first or second bias voltage being output from the bias voltage supply line by turning on the first MOS transistor or second MOS transistor. No such feature is taught or suggested by Koga in the combination as claimed.

Claim 4 further limits claim 3 by requiring that said other of the MOS transistors of the logic circuit be a PMOS transistor and the other transistor of said logic circuit be an NMOS transistor. No such feature is taught or suggested by Koga in the combination as claimed.

Claim 6 further limits claim 1 by requiring that one bias voltage be above the threshold voltage of said other of the complementary serially connected MOS transistors and the other bias voltage be below the threshold voltage of said other of the complementary serially connected MOS transistors. No such feature is taught or suggested by Koga in the combination as claimed.

Claim 7 further limits claim 1 by requiring at least one additional logic circuit coupled to the bias voltage supply circuit. No such feature is taught or suggested by Koga in the combination as claimed.

Claim 8 requires, among other features, a logic circuit comprising a first MOS transistor and a second MOS transistor connected in series between the supply line of a power supply voltage and ground potential, a substrate region of said second MOS transistor being permanently coupled to ground potential, the second transistor having a normally lower leakage and driving current than the normal threshold voltage and leakage current of the first MOS transistor. No such feature is taught or suggested by Koga either alone or in the combination as claimed.

Claim 8 further requires a bias voltage supply circuit which selectively supplies a first bias voltage in the operational state or a second bias voltage in the standby state which are different from each other to the substrate region of the first MOS transistor with substantially no bias voltage supplied to the substrate region of the second transistor to raise the threshold voltage and diminish the leakage current of the first MOS transistor in the steady state. No such feature is taught or suggested by Koga either alone or in the combination as claimed.

Claims 9 to 16 depend from claim 8 and therefore define patentably over the applied references for at least the reasons discussed above with reference to claim 8.

Claim 9 further limits claim 8 by requiring that the first MOS transistor be a PMOS transistor and the second MOS transistor be an NMOS transistor. No such feature is taught or suggested by Koga in the combination as claimed.

Claim 10 further limits claim 8 by requiring that the first bias voltage be lower than the second bias voltage. No such feature is taught or suggested by Koga in the combination as claimed.

Claim 11 requires, among other features, a logic circuit comprising a first MOS transistor and a second MOS transistor connected in series between the supply line of a power supply voltage and ground potential, a substrate region of the second MOS transistor being permanently coupled to ground potential, the second transistor having a normally higher threshold voltage than the normal threshold voltage of the first MOS transistor. No such feature is taught or suggested by Koga either alone or in the combination as claimed.

Claim 11 further requires a bias voltage supply circuit which selectively supplies a first bias voltage in the operational state or a second bias voltage in the standby state which are different from each other to the substrate region of the first MOS transistor with substantially no bias voltage supplied to the substrate region of the transistor coupled to the reference voltage source to raise the threshold voltage and diminish the leakage current of the other of the MOS transistors in the standby state. No such feature is taught or suggested by Koga either alone or in the combination as claimed.

Claim 12 further limits claim 8 by requiring that the first bias voltage be lower than the second bias voltage. No such feature is taught or suggested by Koga in the combination as claimed.

Claim 13 further limits claim 8 by requiring that the bias voltage supply circuit include a first MOS transistor connected between a first voltage supply line and a bias voltage supply line and a second MOS transistor connected between a second voltage

supply line and the bias voltage supply line, and the first or second bias voltage be output from the bias voltage supply line by turning on the first MOS transistor or second MOS transistor. No such feature is taught or suggested by Koga in the combination as claimed.

Claim 14 further limits claim 13 by requiring that the MOS transistor of the logic circuit be connected to the first voltage supply line. No such feature is taught or suggested by Koga in the combination as claimed.

Claim 15 further limits claim 14 by requiring that the MOS transistor of the logic circuit and the first MOS transistor and second MOS transistor be PMOS transistors. No such feature is taught or suggested by Koga in the combination as claimed.

Claim 16 further limits claim 15 by requiring that the logic circuit include an NMOS transistor connected between the PMOS transistor and a third voltage supply line. No such feature is taught or suggested by Koga in the combination as claimed.

Claim 28 further limits claim 11 by requiring that one of the bias voltages be above the threshold voltage of the first MOS transistor and the other of the bias voltages be below the threshold voltage of the first MOS transistor. No such combination is taught or suggested by Koga.

In view of the above remarks, favorable reconsideration and allowance are respectfully requested.

Respectfully submitted,

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